MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2018/2019

EEE4166 – DIGITAL INTEGRATED CIRCUIT

(All sections / Groups)

29 MAY 2019
2.30 p.m – 4.30 p.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This examination paper consists of 6 pages with 4 questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Formulas:

Ideal diode equation: $I_D = I_S(e^{\frac{V_D}{\Phi_T}} - 1)$

$$V_T = V_{TO} + \gamma(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|-2\emptyset_F|})$$

saturation:

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

linear:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right)$$

unified model:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DSAT} - \frac{{V_{DSAT}}^2}{2}\right)(1 + \lambda V_{DS})$$

$$t_P = \frac{C_L\frac{V_{SWING}}{2}}{I_{AVG}}$$

$$t_p = 0.69\,R_{eq}C_L$$

$$P_{dyn} = C_L{V_{DD}}^2 f$$

Question 1

(a) Consider a pn junction diode at T = 300 K in which the reverse-bias saturation current, $I_S = 10^{-14}$ A and n = 1.

(i) Determine the diode current for $v_D = +0.70$ V and $v_D = -0.70$ V. [4 marks]
(ii) Explain the secondary effect of a diode, including a sketch of a graph diode current, I_D vs diode voltage, V_D. [6 marks]

(b) An NMOS transistor has aspect ratio W/L = 3/1 which is operating with V_{SB} = 1.6 V, V_{GS} = 2 V and V_{DS} = 3 V. For a minimum sized NMOS transistor the given threshold voltage is, V_{T0} = 0.43 V, $-2\varphi_F$ = 0.8 V, body effect coefficient, $\gamma = 0.4\ \sqrt{V}$ and $k_n' = 115\ \mu A/V^2$. Determine the mode of operation and the drain current, I_D for this transistor.

[6 marks]

(c) Calculate the diffusion capacitance (C_{diff}) for a transistor with given values:

Width W = 3 μm, length $L_S = L_D$ = 2 μm, and constants given as junction capacitance $C_j = 3.2 \times 10^{-4}$ F/m^2 and junction sidewall capacitance $C_{jsw} = 7.2 \times 10^{-10}$ F/m.

[5 marks]

(d) Refer to Figure Q1 below.

(i) Comment on the impact of the device variation on effective length, L_{eff}. [2 marks]
(ii) In your opinion, what is the cause of variations in CMOS devices? [2 marks]

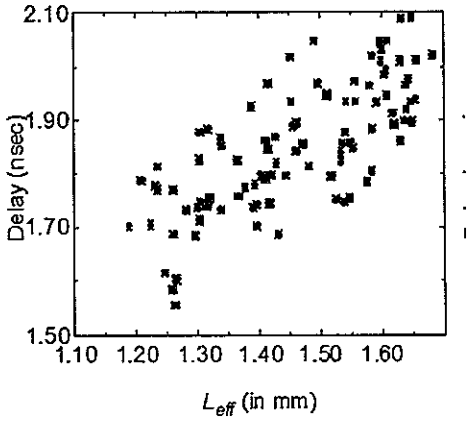

Figure Q1

Continued...

Question 2

(a) Consider a static CMOS inverter.

(i) Describe TWO important properties of static CMOS inverter.

[4 marks]

(ii) Sketch the voltage transfer characteristic (VTC) graph by labelling the axis correctly.

[2 marks]

(iii) Based on the graph drawn in part (ii), label all the critical voltages (V_{OL}, V_{IL}, V_{OH}, V_{IH}) on the graph.

[4 marks]

(iv) State the operating region of the NMOS and PMOS when the input is at V_{IH}.

[2 marks]

(b) Given the function F below:

$$Y = (AB) + \bar{C}$$

(i) Design a static CMOS gate realization of this function F with minimum transistor count. The input and inverted input ports are available for implementation.

[6 marks]

(ii) From the design in Part (i), compute the W/L ratios of the transistors so that the output resistance is the same as that of an inverter with $(W/L)_{NMOS} = 2$ and $(W/L)_{PMOS} = 5$.

[4 marks]

(c) Astable circuit can be used for ono-chip clock generation.
Describe the operation of an oscillator circuit such as a relaxation oscillator.

[3 marks]

Continued...

Question 3

(a) A BJT inverter is shown in Figure Q3(a) below.

(i) **Sketch** a basic BiCMOS inverter and **describe** its operation when the input voltage (VI) applied is LOW. [11 marks]

(ii) Describe THREE features of the BiCMOS inverter. [3 marks]

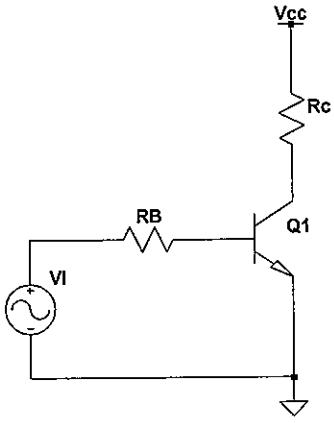

Figure Q3(a)

(b) Design the Emitter-Coupled Logic (ECL) OR/NOR gate of the circuit in Figure Q3(b) below. The desired collector current is I_{C1} = 1.5 mA and V_{EE} = -5 V. At logic high, V_{OR} = -0.7 V, V_{NOR} = -1.6 V and VA = VB = -0.7 V. Assume V_{BE} = 0.7 V.

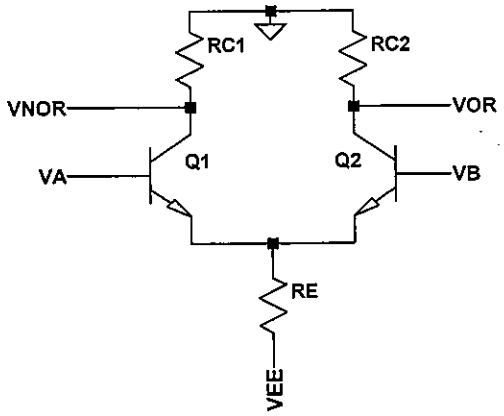

Figure Q3(b)

[11 marks]

Continued...

Question 4

(a) Implement the following functions using static CMOS gates:

(i) $Y = \overline{A.B} + C$ [6 marks]

(ii) $Z = \bar{A} + B.C$ [6 marks]

(b) Based on the circuit implemented in Part (a)(i), determine the dynamic power consumption, P_{dyn} of the circuit, assuming that the load capacitance, C_L = 20 fF, voltage supply, V_{DD} = 3 V and clock frequency, f_{clk} = 150 MHz. Assume that the input signals are random.

Hint: Use a truth table.

[9 marks]

(c) Figure Q4 shows the Power (nW) as a function of Technology Node (nm), simulated on a signal which propagated through one inverter in the middle of an inverter chain with clock frequency of 1 MHz.

(i) Based on Figure Q4, comment on the graph. [2 marks]

(ii) Recommend ONE method to reduce power consumption. [2 marks]

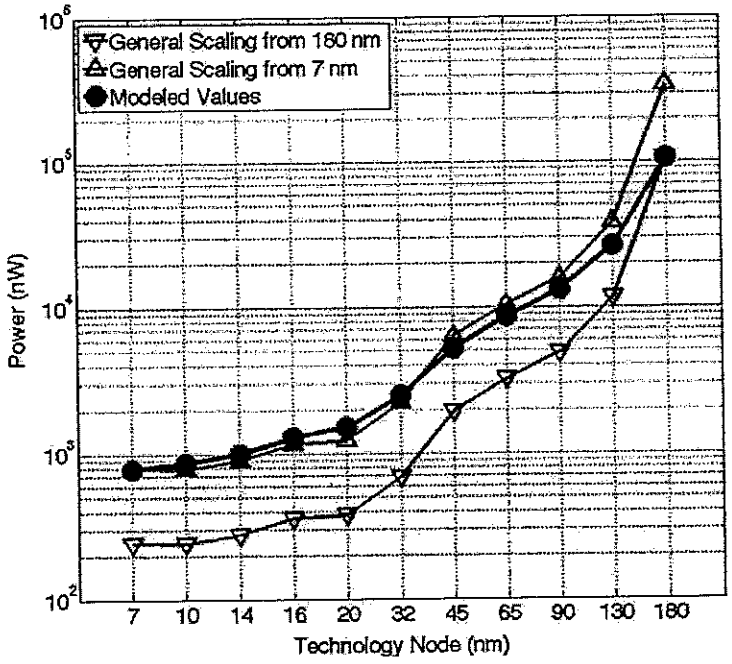

Figure Q4

End of Paper